

257

295

Whitehead
2813

FIG. 1

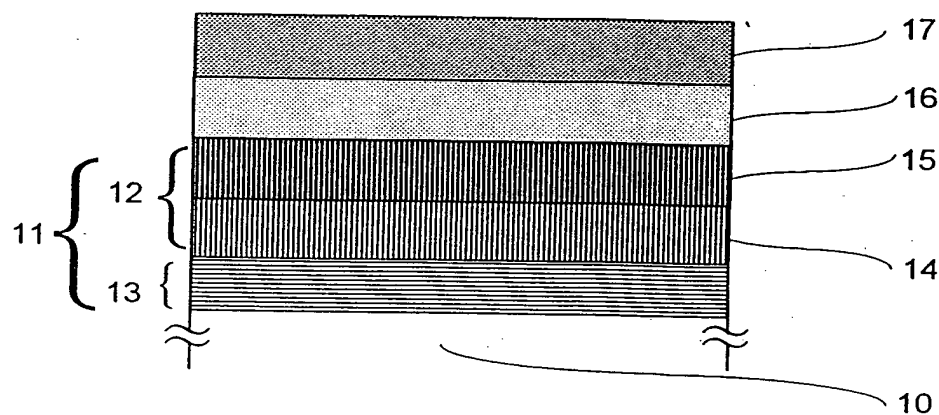


FIG. 2

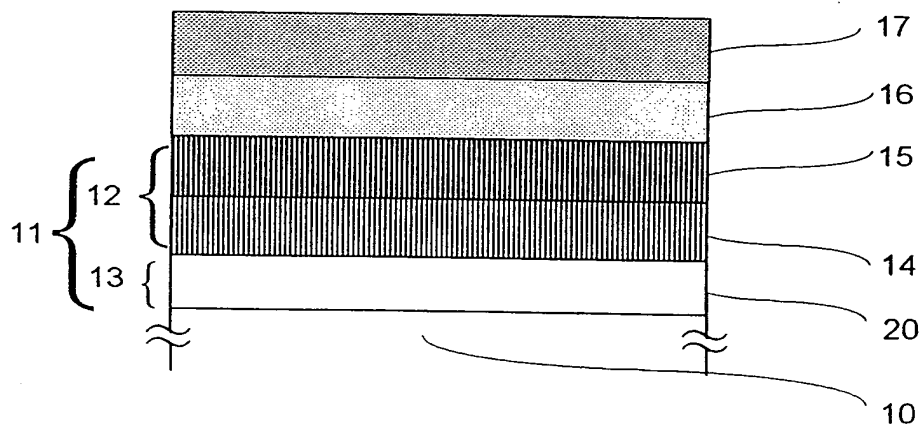


FIG. 3

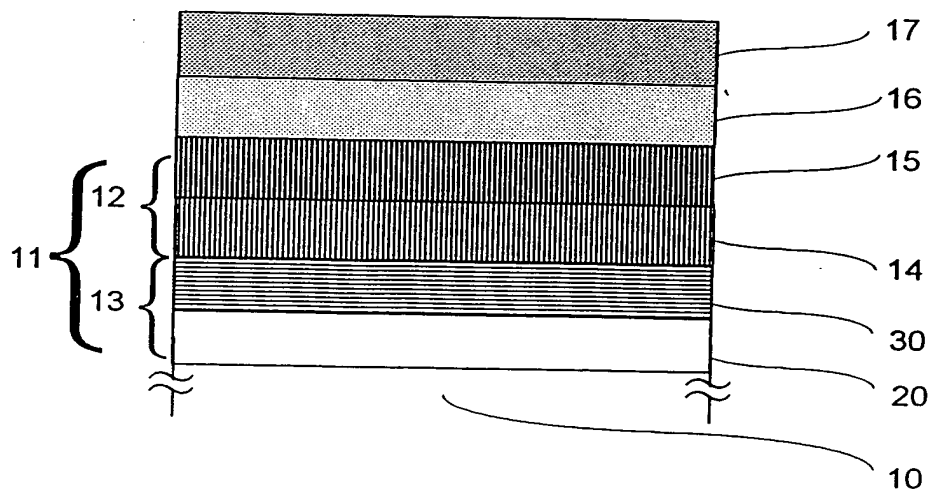


FIG. 4

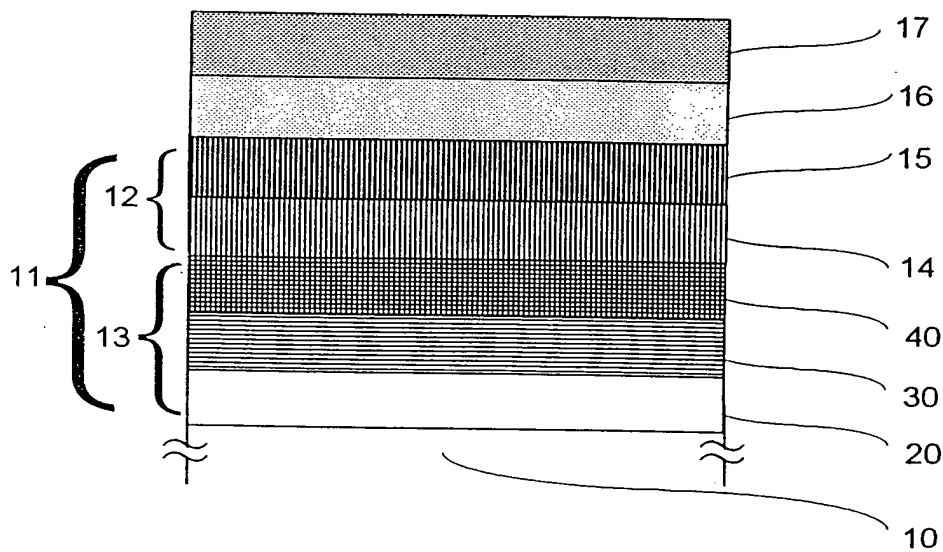


FIG. 5

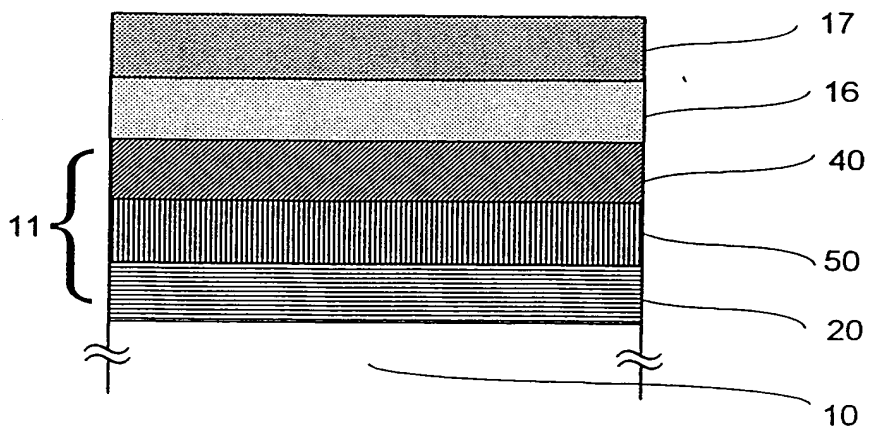
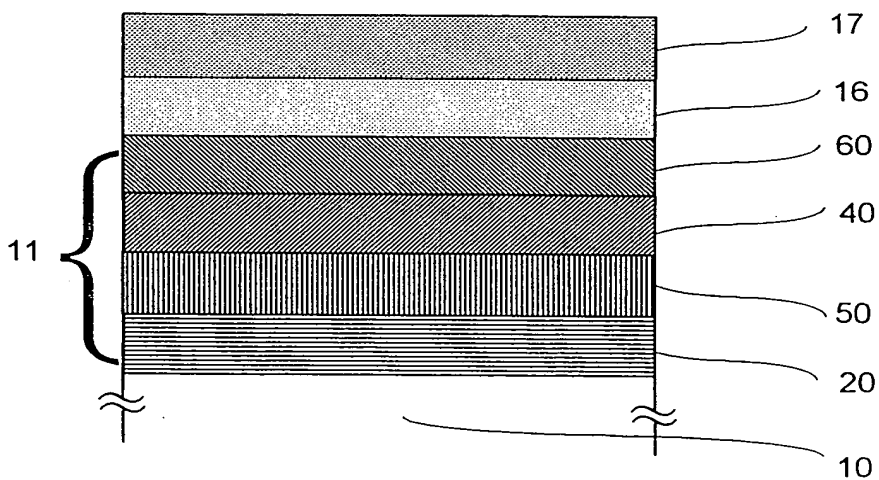


FIG. 6

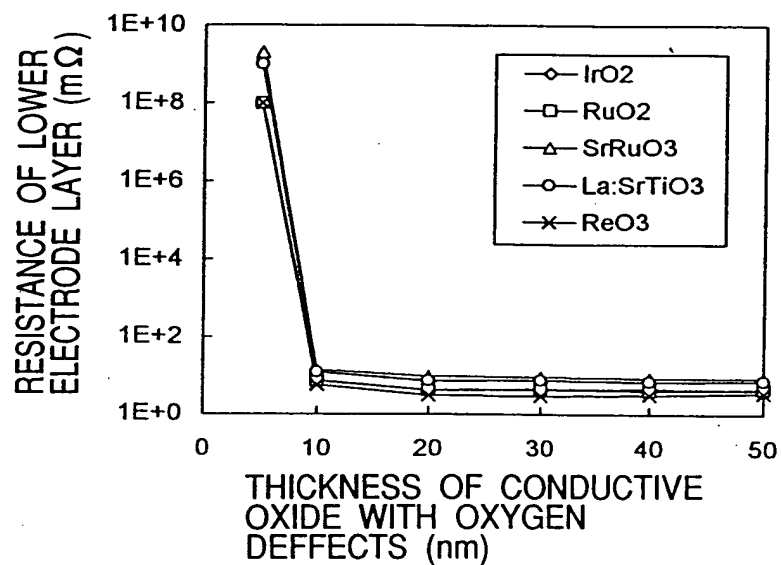


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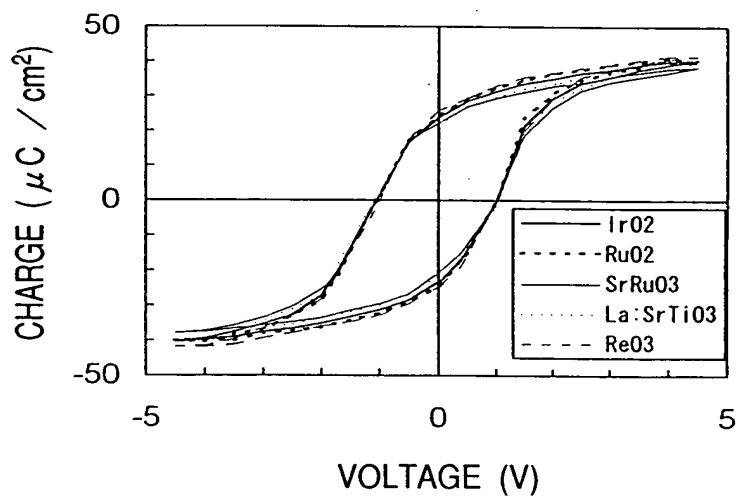
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FIG. 7

(a)



(b)



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FIG. 8

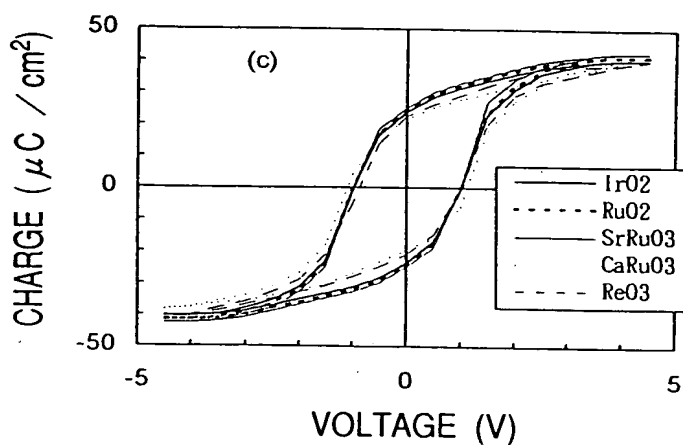
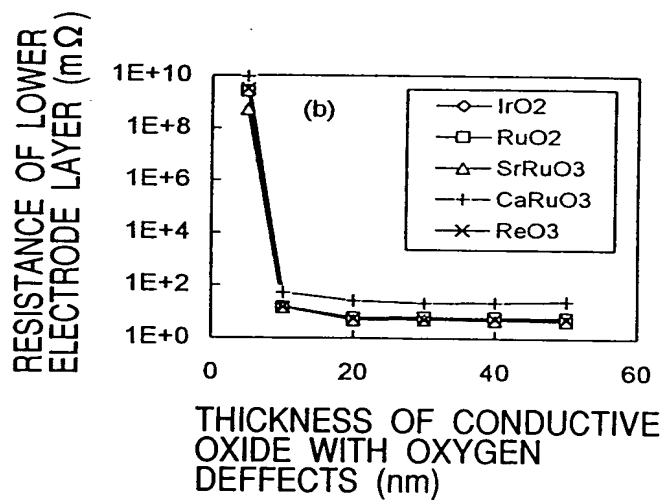
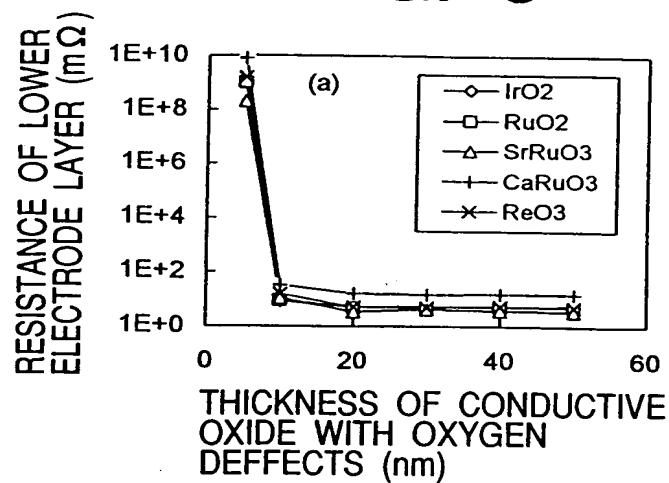
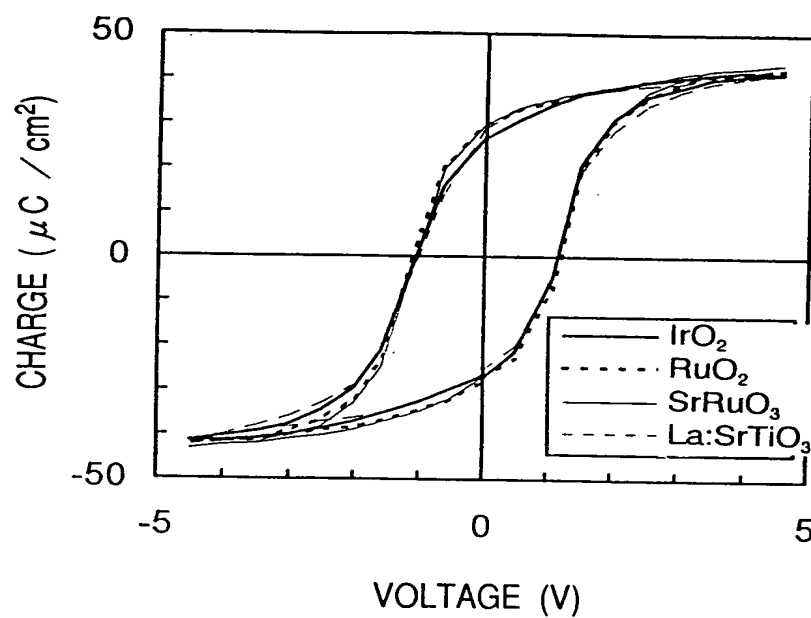
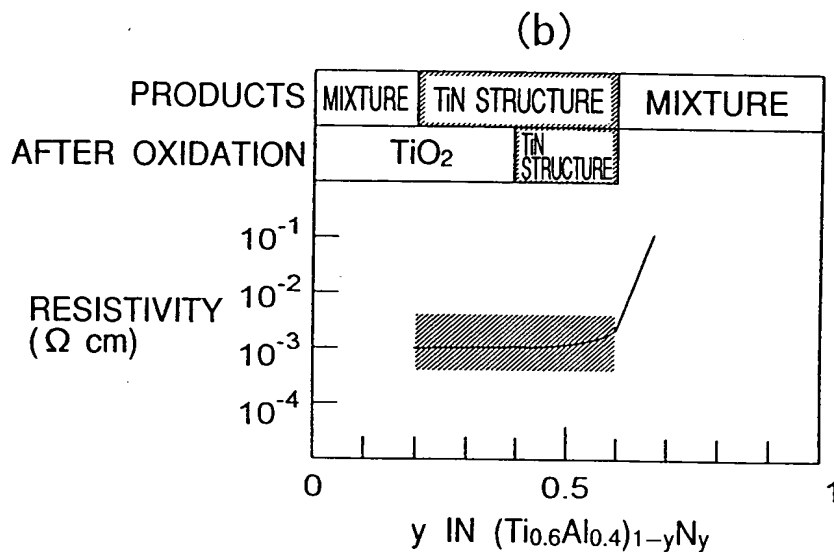
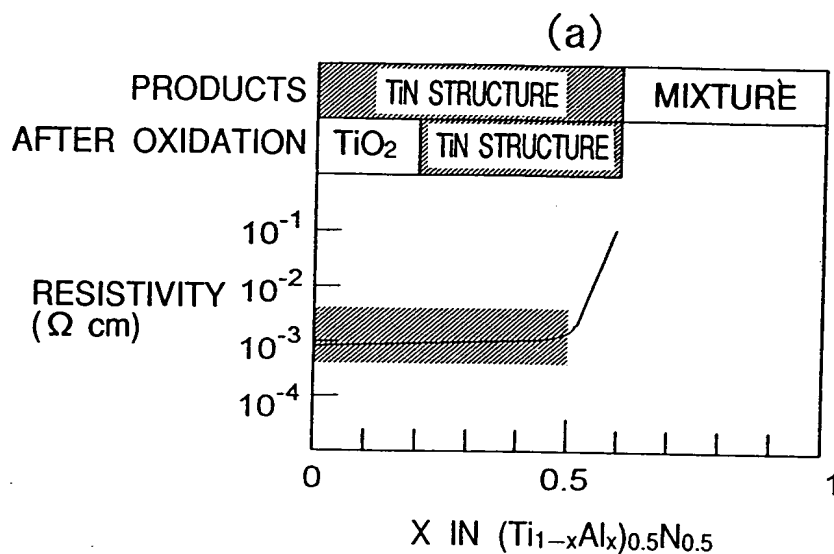


FIG. 9



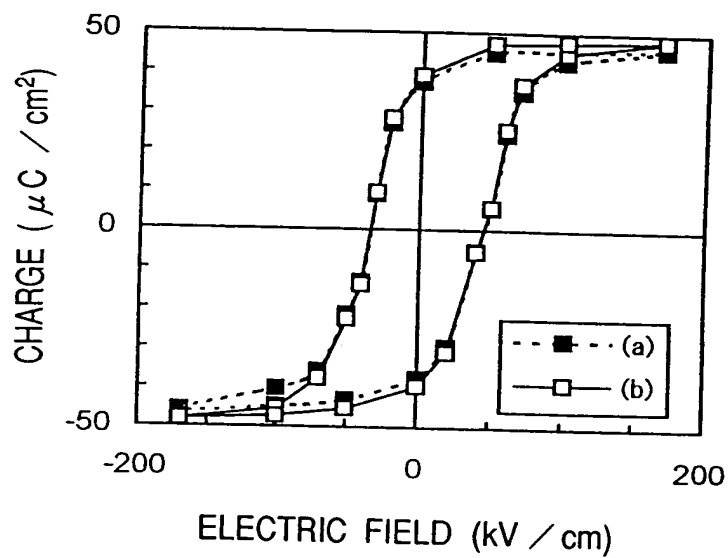
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FIG. 10



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FIG. 11



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FIG. 12

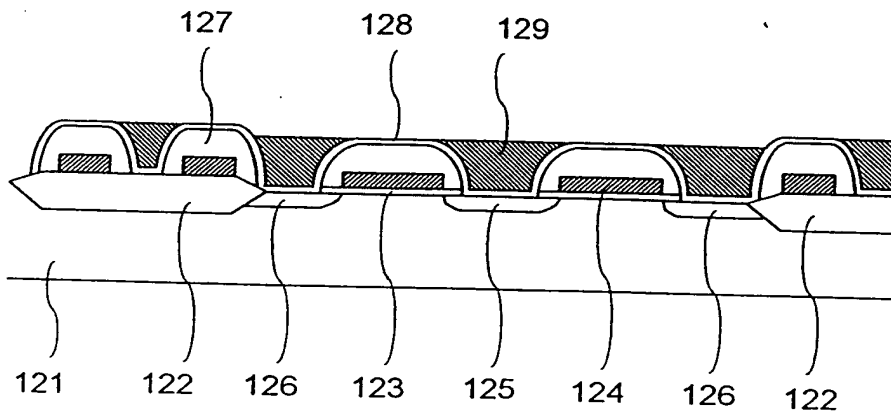
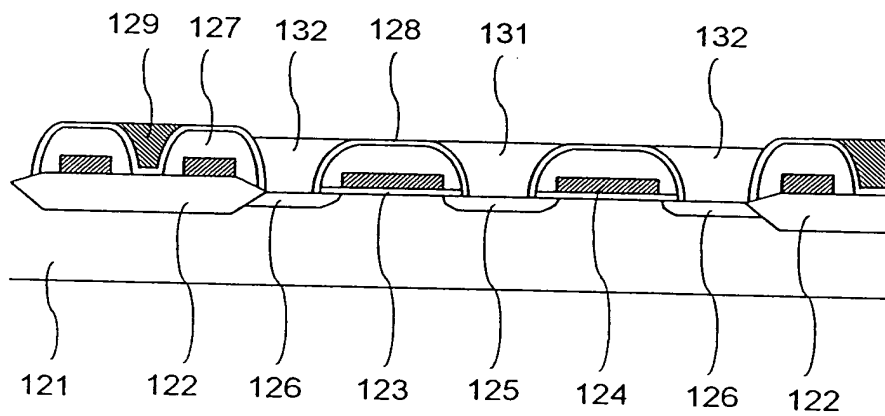


FIG. 13



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FIG. 14

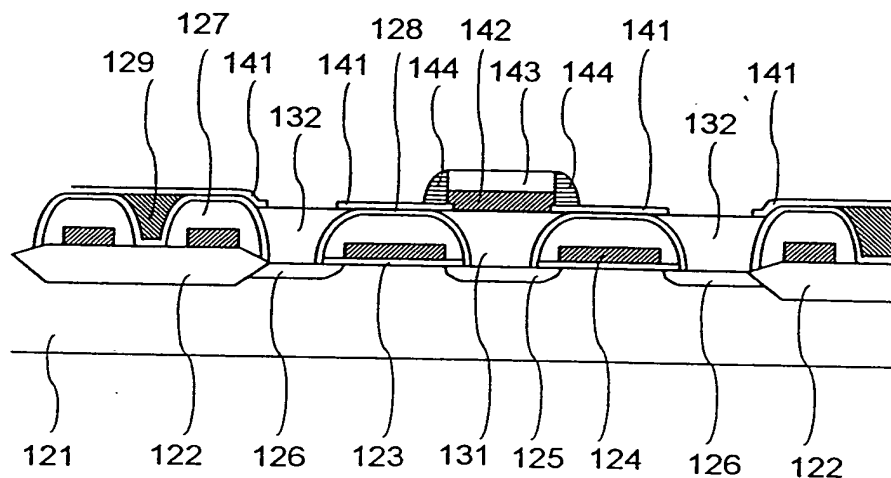


FIG. 15

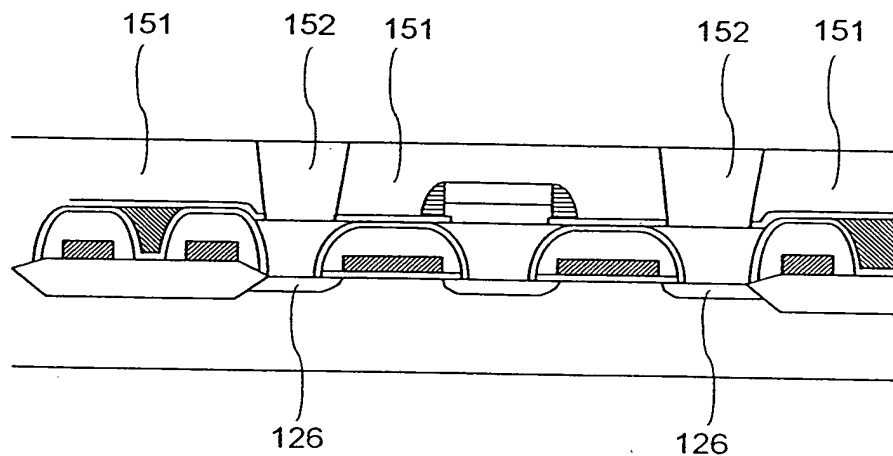


FIG. 16

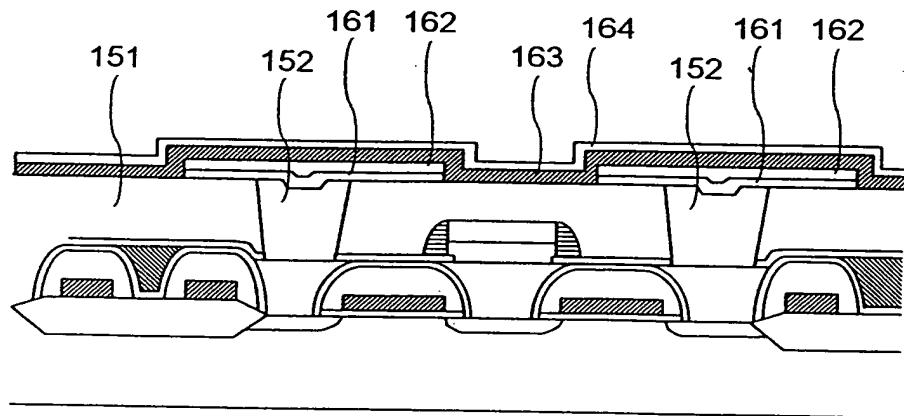
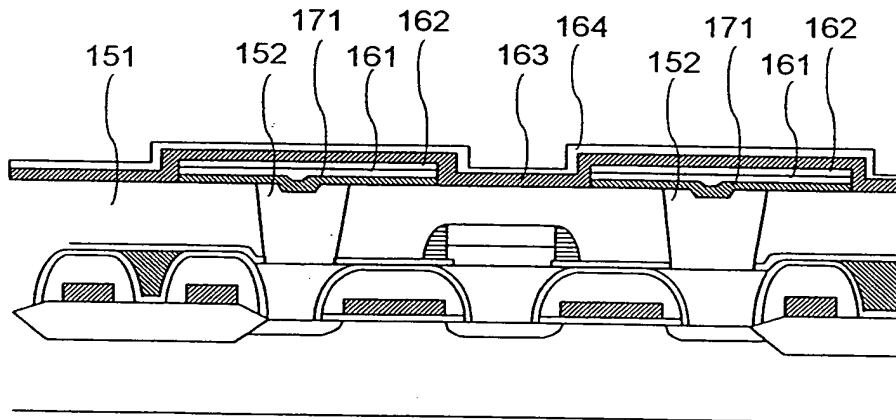
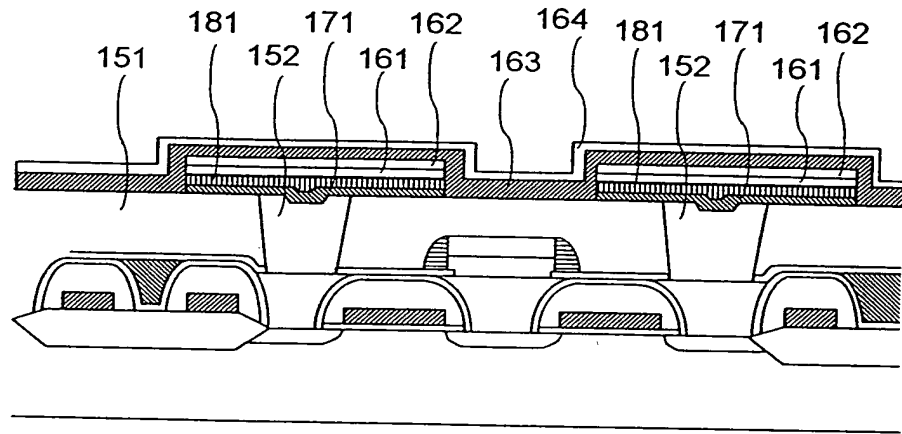


FIG. 17



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FIG. 18



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This diagram shows a cross-sectional view of a second embodiment of the semiconductor device. It features a substrate 151 with a top surface 152. A gate stack 163 is formed on the top surface 152, with a gate dielectric layer 164 on top. The gate stack 163 is divided into gate regions 181 and source/drain regions 191. The source/drain regions 191 are doped with a first impurity and are in contact with the substrate 151. The gate regions 181 are doped with a second impurity and are in contact with the gate dielectric layer 164. The gate dielectric layer 164 is in contact with the top surface 152 of the substrate 151.

This diagram shows a cross-sectional view of a second embodiment of the semiconductor device. It features a substrate with a central raised portion. On the left and right sides of this central portion, there are two sets of semiconductor elements. Each set includes a first semiconductor element (151) and a second semiconductor element (152) stacked vertically. A third semiconductor element (163) is positioned between the two sets of elements. The top surface of the device is covered by a protective layer (181) with openings (191) for the semiconductor elements. A central opening (201) is also present in the protective layer. The central raised portion has a top surface (164) and a side surface (165).